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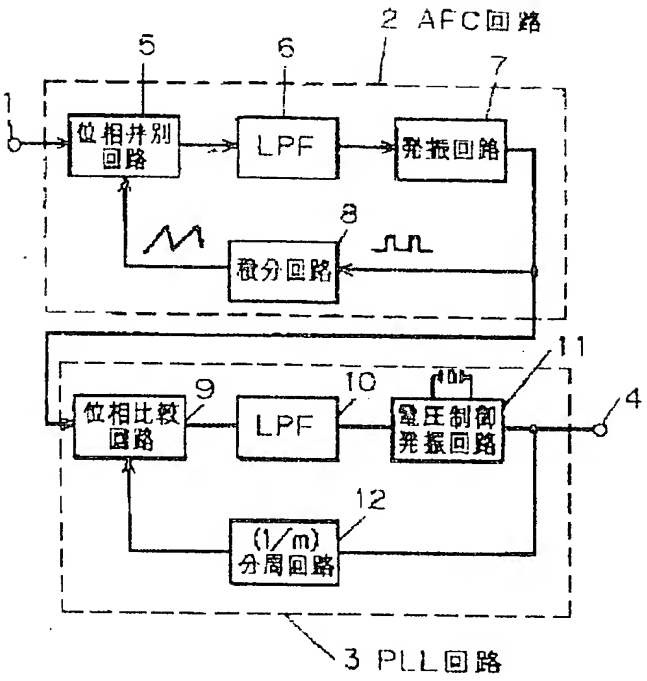
TITLE : SYNCHRONIZING SIGNAL CIRCUIT



ABSTRACT : PURPOSE: To provide a synchronizing signal circuit which can normally construct a PLL even when the input synchronizing signals are omitted or discontinuous.

CONSTITUTION: The omitted input synchronizing signals are supplied through an input terminal 1 and given to an AFC circuit 2 consisting of a phase discrimination circuit 5, an LPF 6, a voltage control oscillation circuit 7 and an integration circuit 8. The circuit 5 integrates the oscillation output signal received from the circuit 7 by the circuit 8 and compares this integrated signal with the input synchronizing signal in terms of levels to detect a phase difference between both signals. Furthermore the circuit 5 is identical with a symmetrical phase discrimination circuit that is balanced to the input synchronizing signal and therefore excels in the resistance to the impulsive noises and the weak electric field characteristic. Thus the output DC potential never extremely varies even if the input synchronizing signal is omitted or supplied to the circuit 5. Therefore the output waveform of the circuit 7 has its frequency and phase approximately equal to those of the input synchronizing signal even when this signal is omitted.